University of California, Santa Barbara
Department of Electrical and Computer Engineering

ECE 152A – Digital Design Principles

Homework #2 – Solution

For problems 1 through 5, include (1) a truth table (for each output), (2) a minimized Boolean expression in either (or both) SOP or POS form and (3) either Karnaugh maps or Boolean algebra demonstrating how the function was minimized.

<u>From Previous Homework:</u>

<u>Problem #1:</u>
Design a combinational circuit with three inputs and one output. The output is equal to logic 1 when the binary value of the input is less than 3. The output is logic 0 otherwise.

Problem #2:
A majority function is generated in a combinational circuit when the output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3-input majority function.
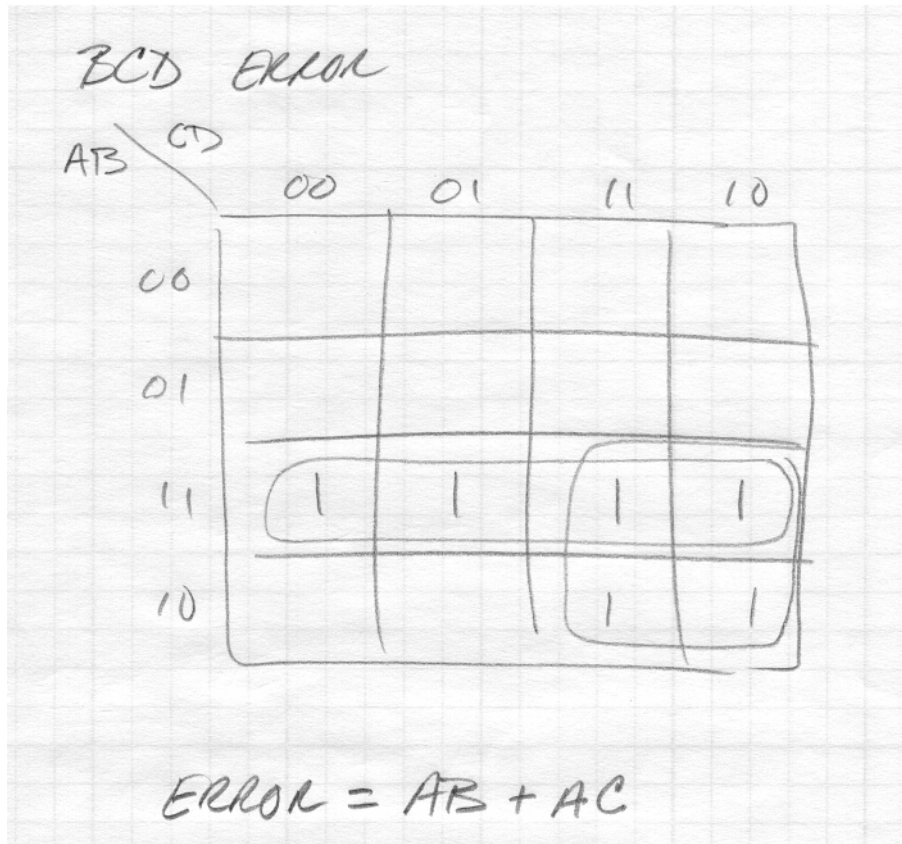

MAJORITY FUNCTION

$$MAJORITY = AC + BC + AB$$

Problem #3:
Design a combinational circuit that detects an error in the representation of a decimal digit in BCD. The output of the circuit must be equal to logic 1 when the inputs contain any one of the six unused bit combinations in the BCD code.

Problem #4:
Design a combinational circuit that produces the binary sum of two, 2-bit
numbers (A1 A0 and B1 B0). The three outputs of this circuit are Carry out (C0),
Sum 1 and Sum 0 (S1 S0).

2 BIT ADDER

A1	A0	B1	B0	C0	S1	S0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

Problem #4 (cont)

$$C_0 = A_1 B_1 + A_1 A_0 B_0 + A_0 B_1 B_0$$

$$S_1 = A_1 B_1' B_0' + A_1 A_0' B_1' + A_1' A_0' B_1 + A_1' B_1 B_0' + A_1' A_0 B_1' B_0 + A_1 A_0 B_1 B_0$$

$$S_0 = A_0 B_0' + A_0' B_0$$

Problem #5:
Design a combinational circuit that multiplies 2, 2-bit numbers (A1 A0 and B1
B0). The four outputs are the four bits of the resulting product (P3 P2 P1 P0).

2 BIT MULTIPLIER

A1	A0	B1	B0	P3	P2	P1	P0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

Problem #5 (cont):

Karnaugh map with rows A1A0 (00, 01, 11, 10) and columns B1B0 (00, 01, 11, 10), with a 1 in row 11, column 11.

$$P3 = A1A0B1B0$$

Karnaugh map with rows A1A0 (00, 01, 11, 10) and columns B1B0 (00, 01, 11, 10), with 1's grouped in the lower right region.

$$P_2 = A1A0'B1 + A1B1B0'$$

Karnaugh map with rows A1A0 (00, 01, 11, 10) and columns B1B0 (00, 01, 11, 10), with 1's circled in groupings.

$$P_1 = A1B1'B0 + A1A0'B0$$
$$+ A1'A0B1 + A0B1B0'$$

Karnaugh map with rows A1A0 (00, 01, 11, 10) and columns B1B0 (00, 01, 11, 10), with 1's grouped in the center.

$$P0 = A0B0$$

From Midterm, Summer 2003

Problem #6.
For the Boolean function given below:

$$F(A,B,C,D) = A'B'C' + A'BC'D' + A'C'D + ACD$$

   (a) Simplify the function (in sum of products representation) using only
        Boolean algebra. Show each step in the simplification.

a) $A'B'C' + A'BC'D' + A'C'D + ACD$

        $A'C'(B' + BD' + D) + ACD$
                    └── OR ──┘ $(x + x'y = x + y)$

        $A'C'(B' + D' + D) + ACD$
                        └─ =1 ─┘

        $A'C' + ACD$

(b) Determine the minimized product of sums representation for the function using only Boolean algebra. You may begin with either the original function or the simplified function derived in part (a). As above, show each step in the simplification.

b) $A'C' + ACD$

$(A' + ACD)(C' + ACD)$

$(A' + CD)(C' + AD)$ $(x + x'y = x + y)$

$(A' + C)(A' + D)(A + C')(C' + D)$

CONSENSUS

OR

CONSENSUS

$(A' + C)(A' + D)(A + C')$

OR

$(A' + C)(A + C')(C' + D)$

Problem #7.
For the function below:

$$F(A,B,C) = AB' + B'C + A'BC'$$
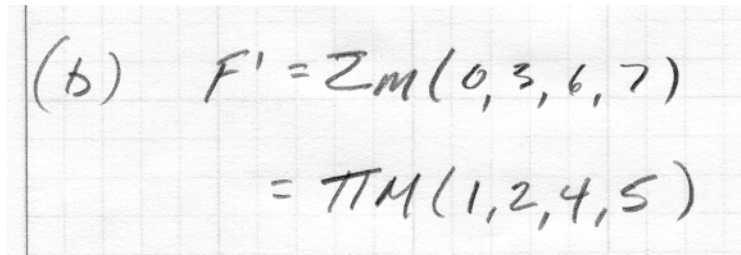
(a) Express the function in sum of minterms (i.e., Σ (*minterm list in decimal form*)) and product of Maxterms (i.e., Π (*Maxterm list in decimal form*)) form.
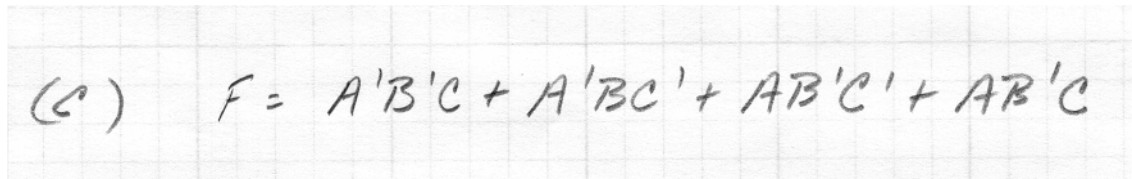
$$AB' + B'C + A'BC'$$

a) $F = \Sigma m(1, 2, 4, 5)$

$\quad = \Pi M(0, 3, 6, 7)$

(b) Express the complement of the function (F') in sum of minterms and product of Maxterms form. Again, the decimal representations of the minterm and Maxterm lists should be used.

$$(b) \quad F' = \Sigma m(0,3,6,7)$$
$$= \Pi M(1,2,4,5)$$

(c) Express the function in standard Sum-of-Products form (i.e., expand minterm abbreviations to product terms)

$$(c) \quad F = A'B'C + A'BC' + AB'C' + AB'C$$

Problem #8.
Implement the following function in minimal Product-of-Sums form using only
NOR gates. Use a Karnaugh map to simplify the function and clearly identify the
grouping of sum terms.

$$F\ (A,B,C,D) = \Sigma\ m\ (2,3,5,7,8,9,10,11,13)$$

$$\Sigma m\,(2,3,5,7,8,9,10,11,13)$$

$$\Pi M\,(0,1,4,6,12,14,15)$$

$$= (B'+D)(A+B+C)(A'+B'+C')$$
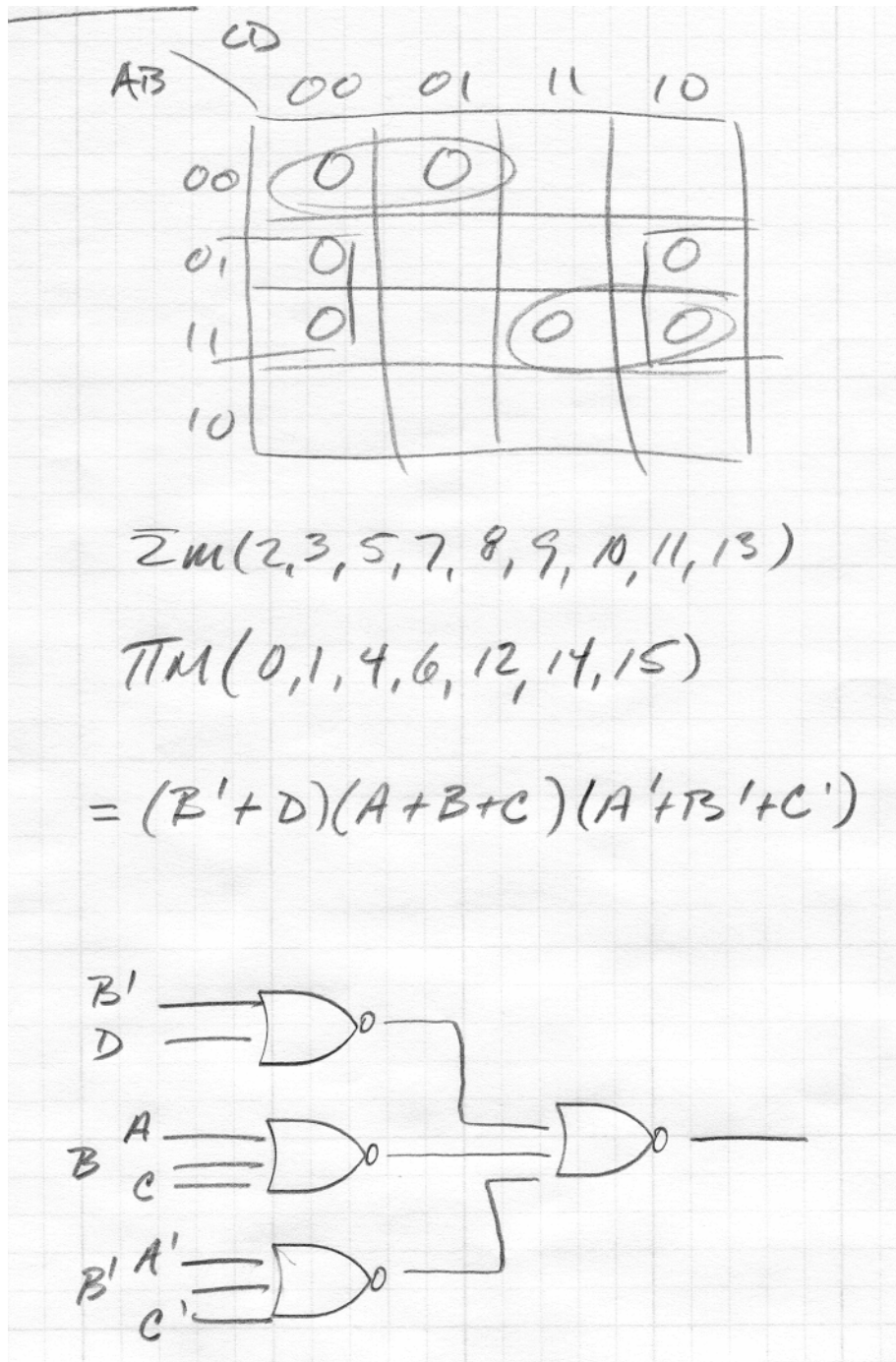
Problem #9.

A standard deck of 52 playing cards is encoded as follows:

S1 S0 = suit	V3 V2 V1 V0 = value
00 Clubs	0001 Ace
01 Diamonds	0010 2
10 Hearts	0011 3
11 Spades	0100 4
	0101 5
	0110 6
	0111 7
	1000 8
	1001 9
	1010 10
	1011 Jack
	1100 Queen
	1101 King

Each card thus has a unique 6 bit encoding, e.g., the Ace of Spades (A♠) is encoded 11 0001, the 9 of Diamonds (9♦) 01 1001, etc.

Design a combinational circuit that takes as its input, the encoding of a single playing card and generates a 1 if that card is an Ace, a 10 or a face card (Jack, Queen or King) and a 0 otherwise. Use the variable names S1 S0 and V3 through V0 for the design.

Your final design should be minimized and in sum of products form. State clearly any assumptions made in constructing the truth table.

ASSUMPTIONS:

① OUTPUT IS A FUNCTION OF VALUE ONLY (NOT SUIT)

② VALUES 0, 14, 15 ARE DON'T CARES

$V3V2$ \\ $V1V0$	00	01	11	10
00	X	1		
01				
11	1	1	X	X
10			1	1

$$= V3V2 + V3V1 + \overline{V3}\,\overline{V2}\,\overline{V1}$$

Problem #10.

Design a combinational circuit that generates an even parity bit for a three bit input word. Recall that the even parity bit is generated in such a way that the total number or ones (the three input bits and the parity bit itself) is even. For example, if the data word is 010, the parity bit would be 1. Conversely, if the data word is 101, the parity bit would be 0.

You are free to use any type of gate in your design.

D2	D1	D0	PARITY (EVEN)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

D2 \ D1D0	00	01	11	10
0		1		1
1	1		1	

$$= D2\,\overline{D1}\,\overline{D0} + \overline{D2}\,\overline{D1}\,D0 + D2\,D1\,D0 + \overline{D2}\,D1\,\overline{D0}$$

or

$$D2 \oplus D1 \oplus D0 \quad (XOR)$$

Problem #11.

In this problem you are to design a 2 bit, shaft position encoder. The shaft rotates clockwise and four sensors provide inputs Q1 Q2 Q3 and Q4 indicating position (quadrant). As the shaft rotates (beginning in quadrant 1), Q1 will be a logic 1 (and all other inputs will be 0). As the shaft enters quadrant 2, input Q2 goes high and some time later, Q1 goes low (Q1 = Q2 = 1 indicates that the shaft is in quadrant 2). Each time the shaft crosses a quadrant boundary, 2 adjacent inputs will be high (temporarily) as shown below.
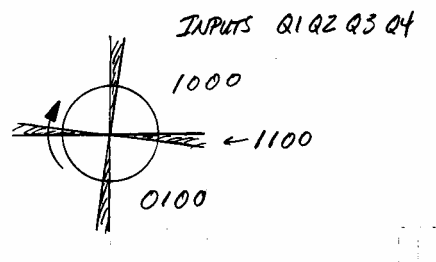
Design a combinational network that generates a 2 bit output indicating the current shaft position. The output of the circuit should be a gray code encoding of the shaft position (P1 P0) with quadrant 1 = 00 (P1 = P0 = 0).

Your final design should be minimized and in sum of products form.

	Q1	Q2	Q3	Q4	P1	P0	
0	0	0	0	0	X	X	
1	0	0	0	1	1	0	Q4
2	0	0	1	0	1	1	Q3
3	0	0	1	1	1	0	(Q4)
4	0	1	0	0	0	1	Q2
5	0	1	0	1	X	X	
6	0	1	1	0	1	1	(Q3)
7	0	1	1	1	X	X	
8	1	0	0	0	0	0	Q1
9	1	0	0	1	0	0	(Q1)
10	1	0	1	0	X	X	
11	1	0	1	1	X	X	
12	1	1	0	0	0	1	(Q2)
13	1	1	0	1	X	X	
14	1	1	1	0	X	X	
15	1	1	1	1	X	X	

GRAY CODE = $00 \rightarrow 01 \rightarrow 11 \rightarrow 10$

$Q1 \rightarrow Q2 \rightarrow Q3 \rightarrow Q4$

$P1 = \overline{Q1}\,\overline{Q2} + Q3$

$P0 = Q2 + Q3\,\overline{Q4}$

From Previous Homework:

Problem #12.
What is the largest binary number that can be obtained with 16 bits? What is its decimal equivalent?

1111 1111 1111 1111

$2^n - 1 = 2^{16} - 1 = 65,535$

Problem #13.
Convert the following binary numbers to decimal:
   1. 101110

$1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 =$
$32 + 0 + 8 + 4 + 2 = \underline{46}$

   2. 1110101.11

$1 \times 2^6 + 1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 +$
$1 \times 2^{-1} + 1 \times 2^{-2} =$
$64 + 32 + 16 + 4 + 1 + ½ + ¼ = \underline{117.75}$

   3. 110110100

$1 \times 2^8 + 1 \times 2^7 + 0 \times 2^6 + 1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 +$
$0 \times 2^1 + 0 \times 2^0 = \underline{436}$

Problem #14.
Convert the following numbers to the indicated bases:

1. Decimal 225 to binary, octal and hexadecimal

    2 | 225   1
    2 | 112   0
    2 | 56   0
    2 | 28   0
    2 | 14   0
    2 | 7   1
    2 | 3   1
    2 | 1   1

    = (1110 0001)$_2$ = (11 100 001)$_2$

    = (E   1)$_{16}$ =   (3   4   1)$_8$

2. Binary 11010111 to decimal, octal and hexadecimal

    $1 \times 2^7 + 1 \times 2^6 + 0 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 =$
    128 + 64 + 16 + 4 + 2 + 1 = 215$_{10}$

    = (1101 0111)$_2$ = (11 010 111)$_2$

    = (D   7)$_{16}$ =   (3   2   7)$_8$

3. Octal 623 to decimal, binary and hexadecimal

    $= 6 \times 8^2 + 2 \times 8^1 + 3 \times 2^0 = 384 + 32 + 1 = 403_{10}$
    = (110 010 011)$_2$ = (1 1001 0011)$_2$ = (1 9 3)$_{16}$

4. Hexadecimal 2AC5 to decimal, octal and binary

    $2 \times 16^3 + 10 \times 16^2 + 12 \times 16^1 + 5 \times 16^0 =$
    8192 + 2560 + 192 + 5 = 10,949$_{10}$

    = (0010 1010 1100 0101)$_2$ = (0 010 101 011 000 101)$_2$
                                    = (0 2   5   3   0   5)$_8$

From Midterm #1, Summer 2005

Problem #15.
For the Boolean equation below:

$$F = A'B + BCD + AC$$

1) Enter the function on a Karnaugh map
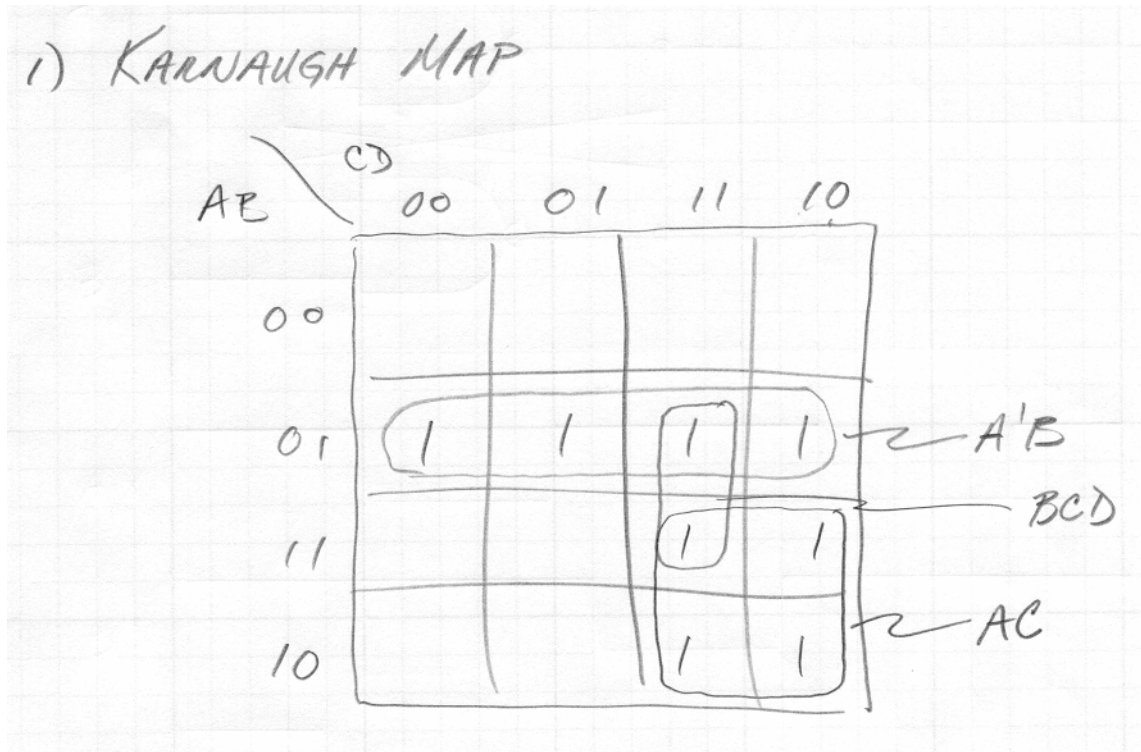
2) Identify and list the prime implicants
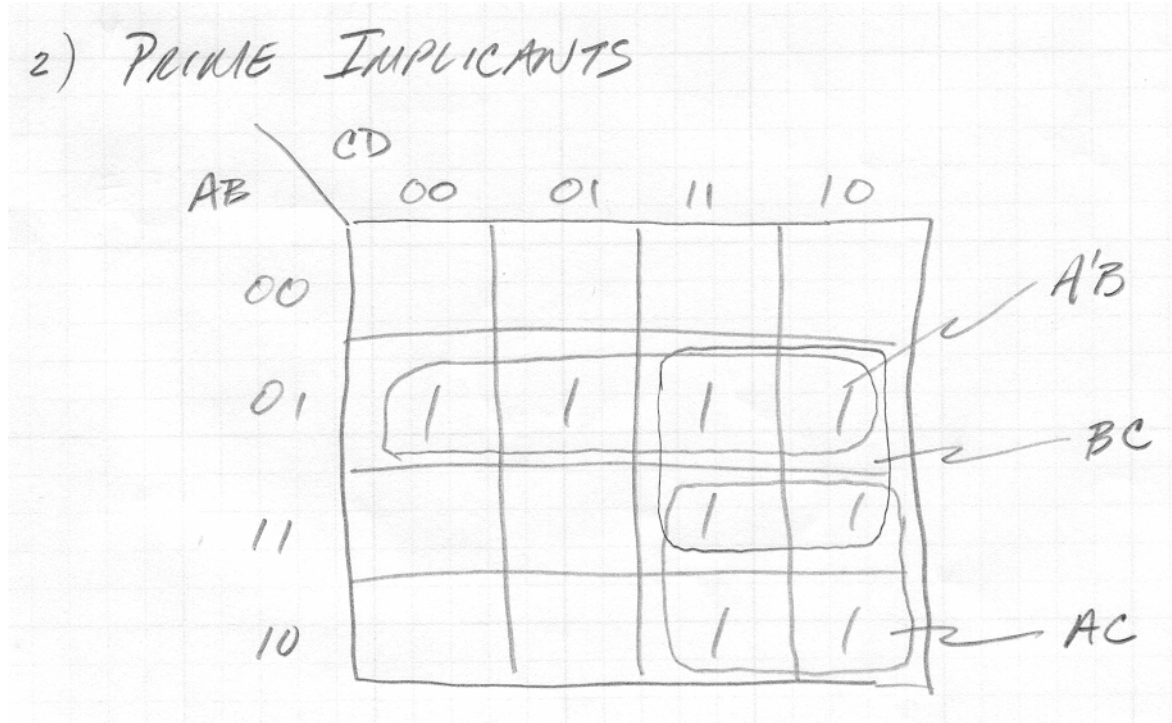
2) PRIME IMPLICANTS

3) Identify and list the essential prime implicants

3) ESSENTIAL PRIME IMPLICANTS

$$A'B, \ AC$$

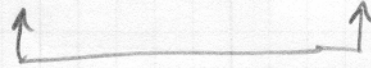4) Determine the minimized Boolean equation from the Karnaugh map

4) MINIMIZED FUNCTION

$$F = A'B + AC$$

5) Simplify the original equation (F = A'B + BCD + AC) using only Boolean algebra and show that it is the same function derived from the Karnaugh map. Show all steps.

5) BOOLEAN SIMPLIFICATION

$$F = A'B + BCD + AC$$

ADD CONSENSUS TERM : BC

$$= A'B + AC + BC + BCD$$

ELIMINATE BCD BY X + XY = X

$$= A'B + AC + BC$$

ELIMINATE CONSENSUS TERM

$$= A'B + AC$$

Problem #16.
For the function indicated on the Karnaugh map below, provide the following:

AB\CD	00	01	11	10
00	0	1	0	0
01	1	1	1	1
11	0	1	1	0
10	0	1	0	0

1) The minimized function in sum of products representation

1) SUM OF PRODUCTS

$$F = A'B + BD + C'D$$

2) The minimized function in product of sums representation

2) PRODUCT OF SUMS

$$F = (B+C')(A'+D)(B+D)$$

3) Using only Boolean algebra, convert the minimized sum of products representation to product of sums representation

3) SOP ⟶ POS

$$A'B + BD + C'D$$

$$(A'B + B)(A'B + D) + C'D$$

$$(B)(A' + D)(B + D) + C'D$$

$$((B)(A' + D) + C')((B)(A' + D) + D)$$

$$(B + C')(A' + D + C')(B + D)(A' + D + D)$$

$$(B + C')(B + D)(A' + D)$$

4) Using only Boolean algebra, convert the minimized product of sums representation to sum of products representation

4) POS → SOP

$$(B+C')(A'+D)(B+D)$$

$$\underline{\begin{array}{l} B+C' \\ A'+D \end{array}}$$

$$A'B + A'C' + BD + C'D$$

$$\underline{B + D}$$

$$A'BB + A'BC' + BBD + BC'D +$$

$$A'BD + A'C'D + BDD + C'DD$$

$$= A'B + BD + C'D$$

Problem #17.
For the function expressed below in sum of minterm representation:

$$F(A,B,C,D) = \Sigma_m (0,5,7,8,15) + d(2,3,6,10,14)$$

1) Express the function in product of Maxterm representation

1) MAXTERM REPRESENTATION

$$F(A,B,C,D) = \Pi_M(1,4,9,11,12,13) \cdot d(2,3,6,10,14)$$

2) Express the complement of the function (F') in sum of minterm representation

2) COMPLEMENT (F')

$$F'(A,B,C,D) = \Sigma_m(1,4,9,11,12,13) + d(2,3,6,10,14)$$

3) Using a Karnaugh map, minimize the original function (F) in sum of products representation.

$$F = A'BD + BC + B'D'$$

Problem #18.
Construct a logic network that realizes the three input OR function (A + B + C) using only two input NAND gates (AB)'.

Prove that your design works correctly by annotating the output of each NAND gate with its Boolean equation.

FIRST MAKE A 2 INPUT OR GATE

$$A + B = ((A+B)')' = (A' \cdot B')'$$

$$(A' \cdot B')' = A + B$$

NEXT, BECAUSE A+B+C = (A+B) + C

A+B

$$(A' \cdot B')$$

$$c'$$

$$(A' \cdot B' \cdot C')'$$

$$= (A + B + C)$$
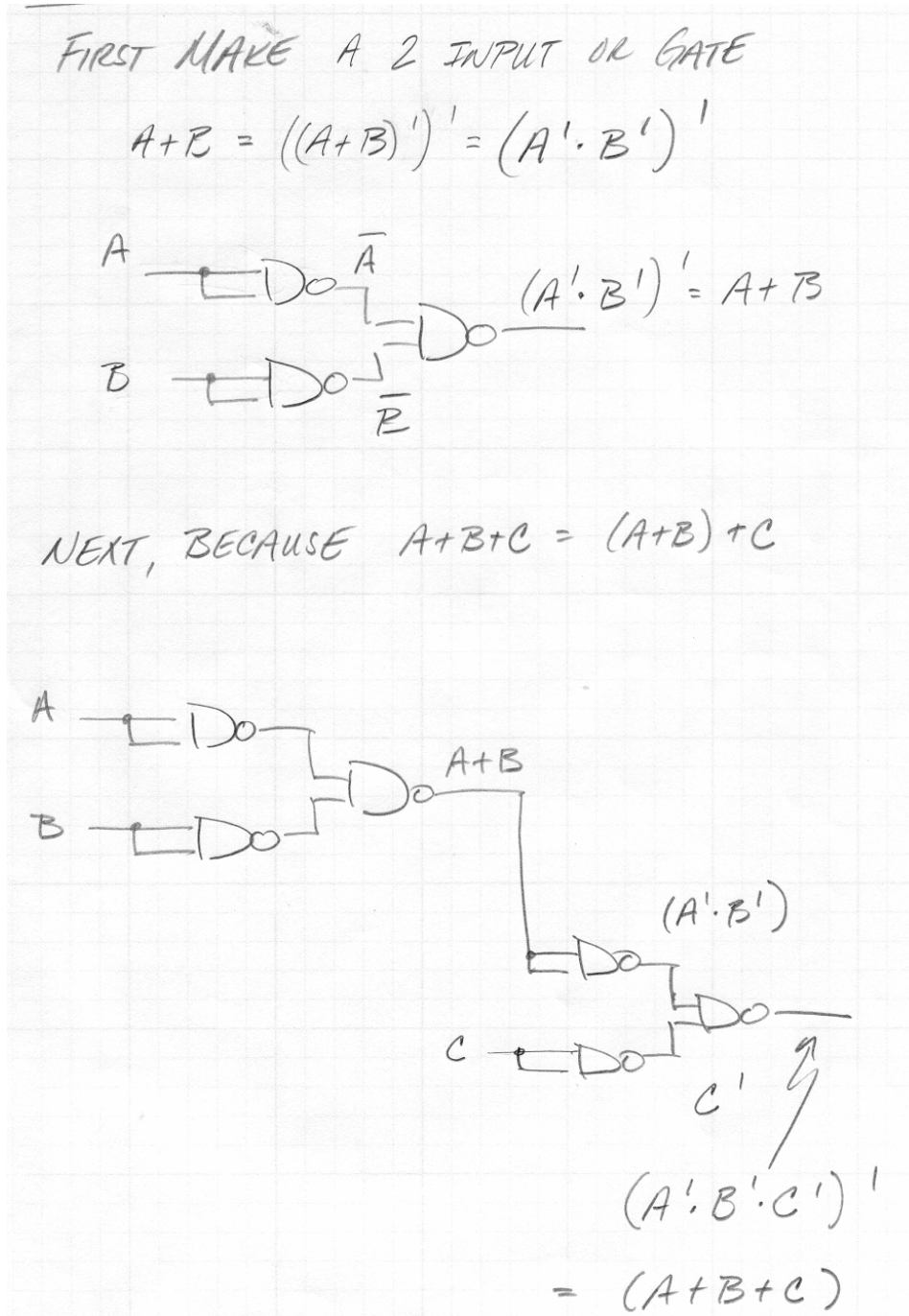
Problem #19.

A data selector is a combinational circuit that selects (i.e., places at the output) one data input from a number of data inputs. In this problem you are to design a data selector with two data inputs (A and B) and two control inputs, select (SEL) and enable (EN). When EN is low, the output should be low regardless of the value of the data inputs or the SEL input. When EN is high and SEL is low, the A data input should appear at the output; Conversely, when EN is high and SEL is high, the B data input should appear at the output.

Implement your design using only NOR gates. Include:

1) The Karnaugh map
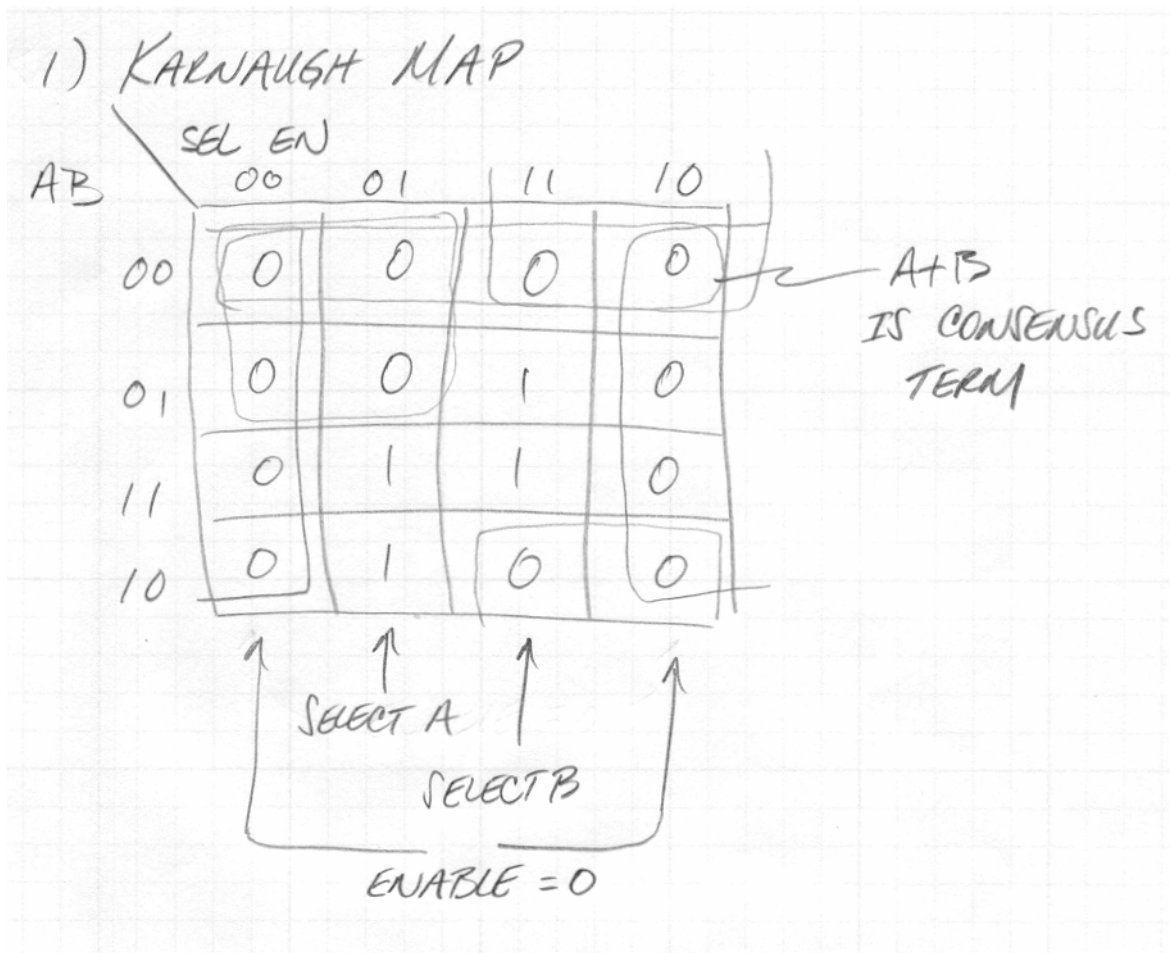
2) The simplified Boolean equation in product of sums format

2) BOOLEAN EQUATION

$$Z = EN \cdot (A+S)(B+\bar{S})$$

3) A logic diagram of the complete implementation
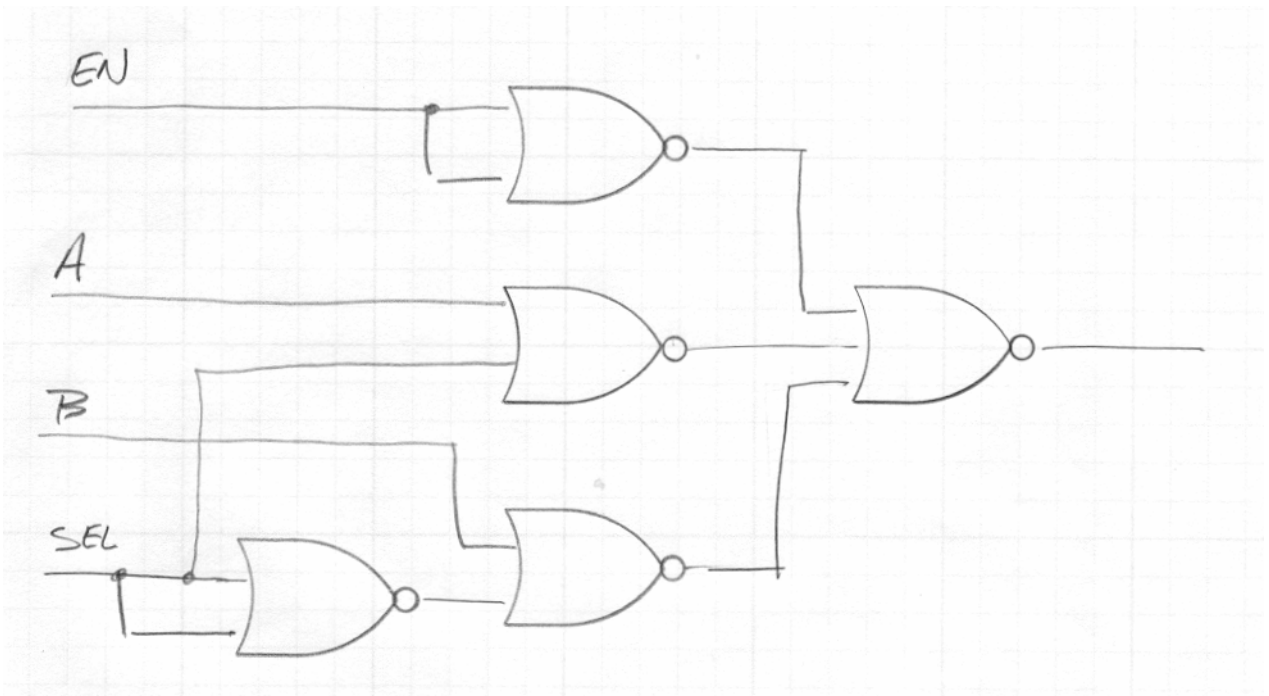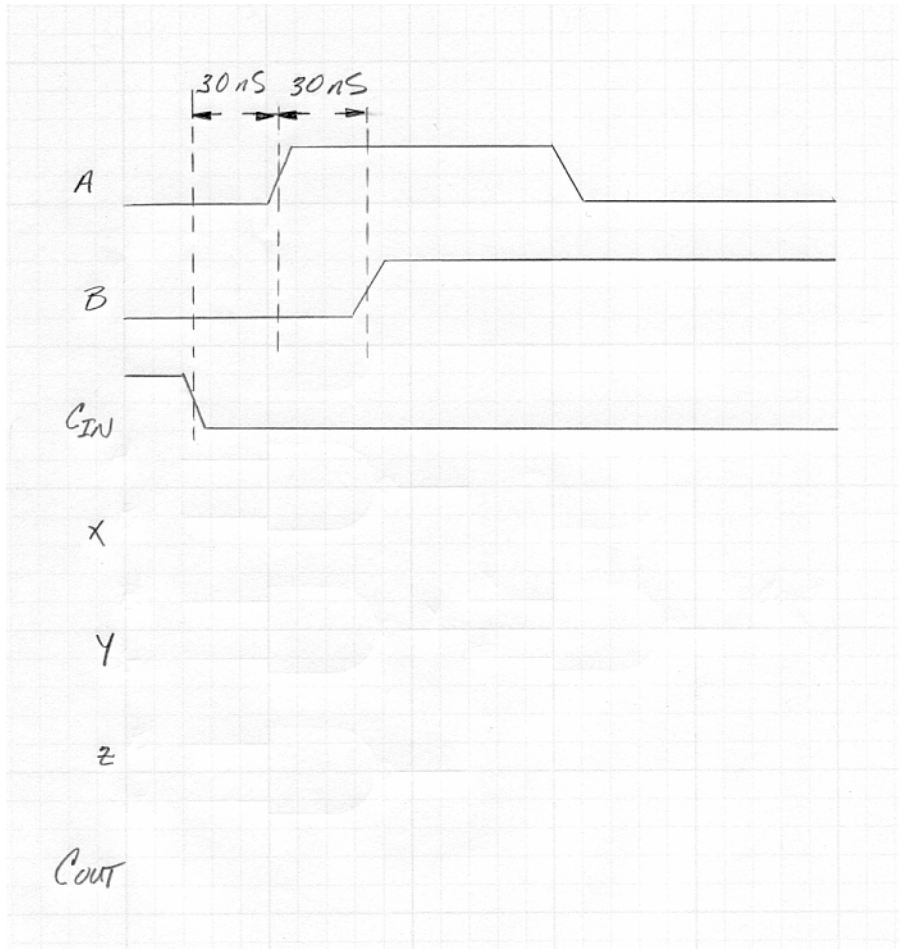
Problem #20.
The logic diagram below illustrates the implementation of the Carry Out function
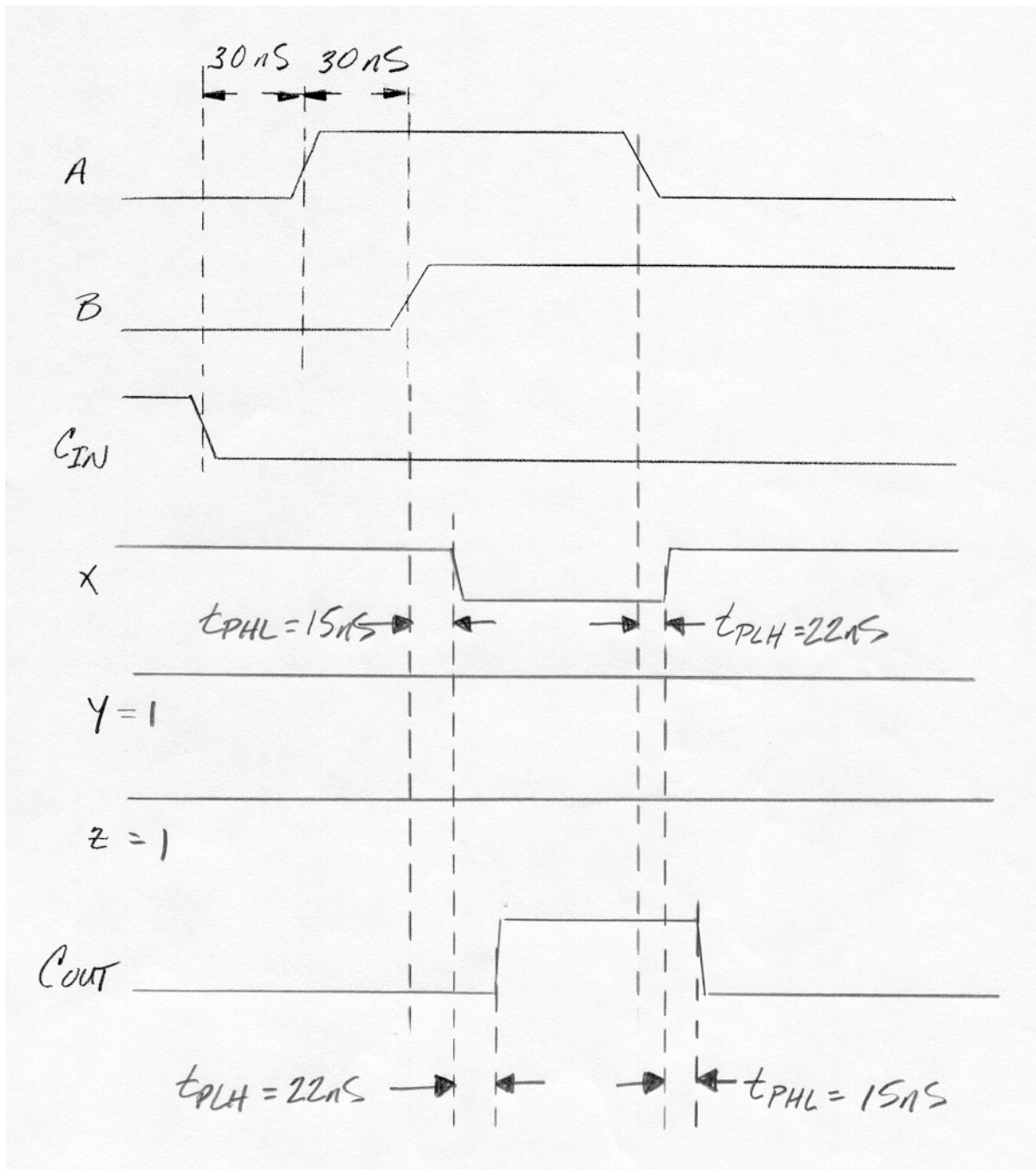of a full adder.
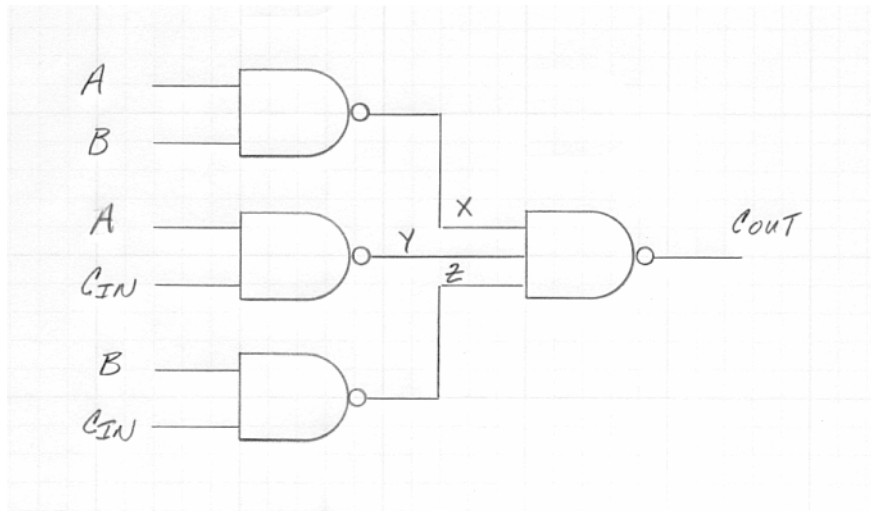
The data sheets for both the 2 input NAND gate (7400) and the 3 input NAND
gate (7410) list the following propagation delays:

$$t_{PLH} = 22 \text{ ns and } t_{PHL} = 15 \text{ ns}$$

Complete the timing diagram below. Indicate all relevant propagation delays on the timing diagram

From Midterm #1, Summer 2004:

Problem #21.

Using only Boolean algebra and showing all steps:

1) Convert the following expression to product-of-sums representation:

A'BC + AB'

(1) A'BC + AB'

(A' + AB')(B + AB')(C + AB')

(A' + A)(A' + B')(A + B)(B + B')(A + C)(B' + C)

(A' + B')(A + B)(A + C)(B' + C)

CONSENSUS TERMS (B' + C) OR (A + C)

CAN BE ELIMINATED (BUT NOT BOTH)

2) Convert the following expression to sum-of-products representation:

$$(A + B)\ (A + C)\ (A' + B')$$

(2) $(A + B)(A + C)(A' + B')$

$A + B$
$A + C$
_____
$A + AB$
$\quad + AC + BC$

$A + BC$

$A' + B'$
_____
$AA' + A'BC +$ $= A'BC + AB'$

$\quad AB' + B'BC$

Problem #22.

1) Prove (using only Boolean algebra) that the following expression is true.

$$(A + B' + C)(A + B' + C')(A + B' + D') = A + B'$$

(1) $(A + B' + C)(A + B' + C')(A + B' + D') = A + B'$

              $= (A + B')$;

                  $(A + B')(A + B' + D')$

                      $= A + B'$

2) What is the dual of the expression above?

(2) $AB'C + AB'C' + AB'D' = AB'$ (DUAL)

3) Prove (using any valid technique) that the dual is also true.

(3)   SINCE EXPRESSION IS TRUE, DUAL
       IS ALSO TRUE

Problem #23.

Find the minimal sum-of-products representation for the function:

$$Z = [(A + B') ' C' + A B C] '$$

$$Z = [(A+B')' C' + ABC]'$$

$$= [A'BC' + ABC]'$$

$$= (A+B'+C)(A'+B'+C')$$

MAP POS, GROUP 1's FOR SOP

A \\ BC	00	01	11	10	
0	1	1	1	0	(A+B'+C)
1	1	1	0	1	AC'

B'

(A'+B'+C')

$$Z = B' + AC' + A'C$$

Problem #24.

Design a combinational network that detects overflow in the 2's complement addition of two, 8-bit numbers and generates an output of 1. The two operands should be represented as A7 – A0 and B7 – B0, with A7 and B7 being the most significant bits. The sum is represented as S8 – S0 with S8 the carry out of the adder and S7 the most significant bit of the sum. Implement your design in standard sum-of-products representation using ANDs, ORs and INVERTERS.

2'S COMPLEMENT OVERFLOW OCCURS
WHEN 2 POSITIVE NUMBERS ARE ADDED
AND YOU GET A NEGATIVE RESULT, OR
2 NEGATIVE NUMBERS ARE ADDED
AND YOU GET A POSITIVE RESULT
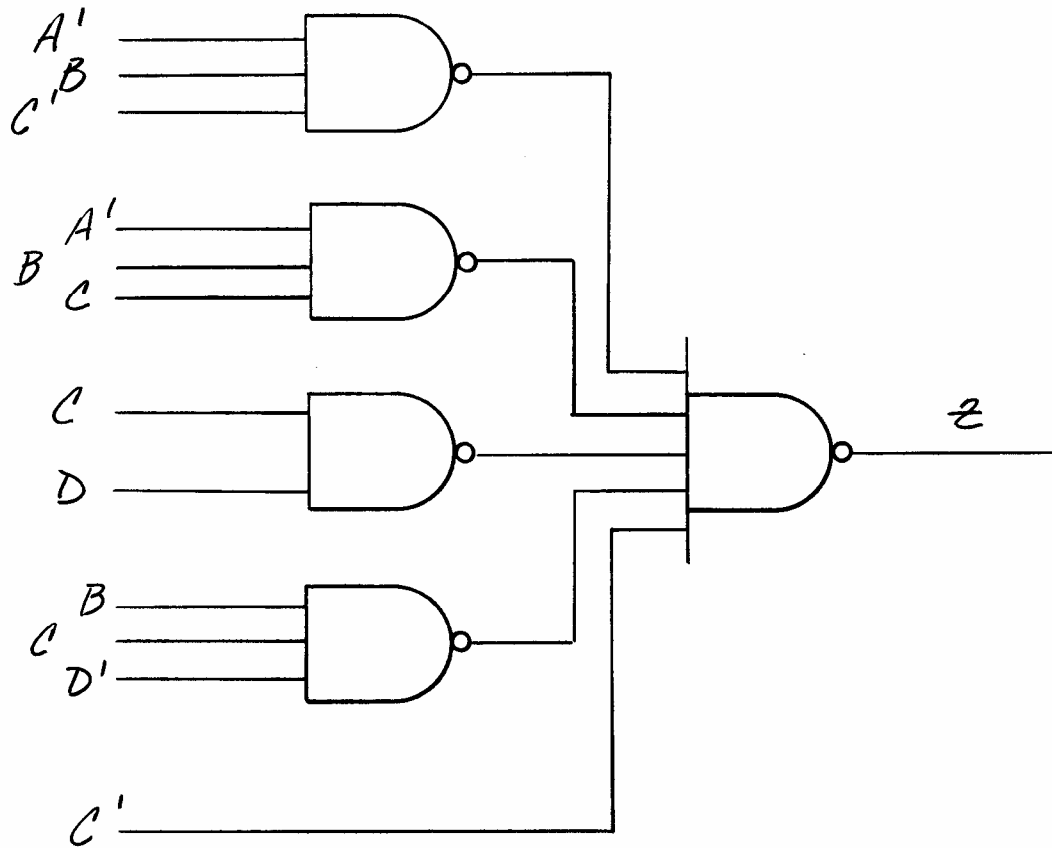
$\Rightarrow$ YOU ONLY HAVE TO LOOK AT
THE SIGN BITS

S_7 \ $A_7 B_7$	00	01	11	10
0			1	
1	1			

$$Z = S_7 A_7' B_7' + S_7' A_7 B_7$$

Problem #25.

For the logic network shown below:

1) Construct a Karnaugh map

YOU CAN DO THIS BY INSPECTION, OR
WORK THROUGH THE NAND GATES

$$\left[(A+B'+C)(A+B'+C')(C'+D')(B+C'+D)(C') \right]'$$

$$= A'BC' + A'BC + CD + BCD' + C$$

(1) MAP THE TERMS:

2) Find the minimal sum-of-products representation

(2) SOP: $A'B + C$

3) Find the minimal product-of-sums representation

(3) POS: $(A'+C)(B+C)$

Problem #26.

This problem requires you to design a combinational network that implements an alarm system. There are 3 inputs to the alarm: door locked, door open and window open. The door and window can only be opened if the door is unlocked. The network should generate an alarm if either the door or the window is open. Implement the function in standard sum-of-products form.

THIS NETWORK HAS SOME DON'T CARES
BECAUSE THE DOOR AND WINDOW
CAN NEVER BE OPENED IF THE DOOR
IS LOCKED

L = DOOR LOCKED

W = WINDOW OPEN

D = DOOR OPEN

| L \ WD	00	01	11	10
0	0	1	1	1
1	0	X	X	X

$$Z = W + D$$

Problem #27.

For the function:

$$F = \Sigma_m (0,1,2,6,7,11,12,13,14,15)$$

1) Identify all of the prime implicants by constructing a Karnaugh map, grouping them on the map and listing them in product term form. Use the variable names A, B, C and D where A'B'C'D' = minterm 0.

2) Identify the essential prime implicants.

3) What is the minimal sum-of-products representation?

4) Is the minimal sum-of-products representation unique (why or why not)?

$$\Sigma_m = (0, 1, 2, 6, 7, 11, 12, 13, 14, 15)$$
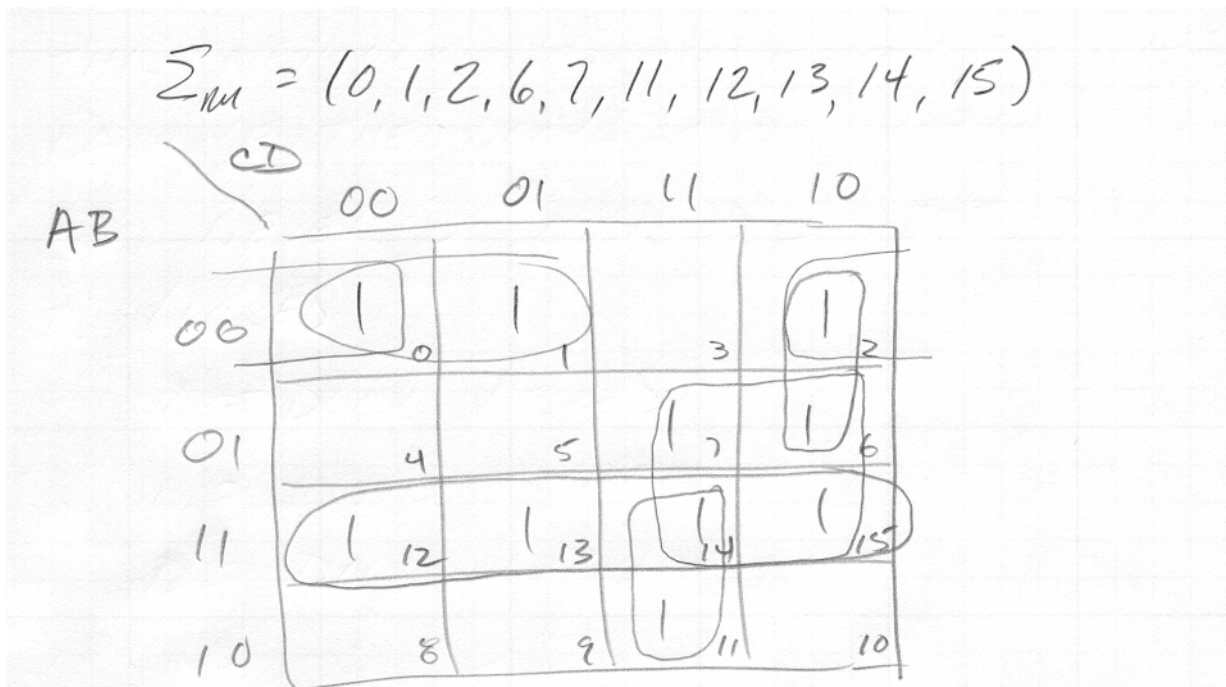
PRIME IMPLICANTS

AB, BC, ACD, $A'CD'$, $A'B'D'$, $A'B'C'$

ESSENTIAL PRIME IMPLICANTS

$AB + BC + ACD + A'B'C' + \begin{cases} A'CD' \\ OR \\ A'B'D' \end{cases}$

IT IS NOT UNIQUE BECAUSE EITHER
SOLUTION IS MINIMAL

Problem #28.

For the function:

$$F = (A + B) (B' + C' + D) (A' + B + C + D') (C' + D)$$

1) Express the function in Product of Maxterm representation.

2) Express the function in Sum of Minterm representation

3) Express the complement of the function in Product of Maxterm representation

4) Express the complement of the function in Sum of Minterm representation

You are free to use any technique (i.e., Boolean algebra, K-map, truth table) to solve this problem.

$$(A+B)(B'+C'+D)(A'+B+C+D')(C'+D)$$

MAP THE PRODUCT OF SUMS

(1) $F = \prod M(0,1,2,3,6,9,10,14)$

(2) $F = \sum_m (4,5,7,8,11,12,13,15)$

(3) $F' = \prod M(4,5,7,8,11,12,13,15)$

(4) $F' = \sum_m (0,1,2,3,6,9,10,14)$

From Midterm #1, Summer 2006:

Problem #29.

(1) Using only Boolean algebra, Convert the following expression to standard sum of products form.

$$F = (A + B'C + B'D') (B + C' + D) (A' + B + C')$$

$$F = (A+B'C + B'D')(B+C'+D)(A'+B+C')$$

$$B + C' + D$$

$$\overline{}$$

$$AB + BB'C + BB'D'$$
$$+ AC' + B'CC' + B'C'D'$$
$$+ AD + B'CD + B'D'D$$

$$= AB + AC' + B'C'D' + AD + B'CD$$

$$A' + B + C'$$
$$\overline{}$$

$$AA'B + AA'C' + A'B'C'D' + A'AD + A'B'CD$$
$$+ AB + ABC' + BB'C'D' + ABD + BB'CD$$
$$+ ABC' + AC' + B'C'D' + ACD$$
$$+ B'CC'D$$

$$= AB + AC' + B'C'D' + A'B'CD$$

(2) Using only Boolean algebra, convert the above expression to standard product of sums form.

$$(2) \quad F = \overline{(A + B'C + B'D')}(B + C' + D)(A' + B + C')$$

$$= A + B'(C + D')(B + C' + D)(A' + B + C')$$

$$= (A + B')(A + C + D')(B + C' + D)(A' + B + C')$$

(3) Verify both results by constructing a Karnaugh map and identifying the sum and product terms from the expressions in parts (1) and (2) above.
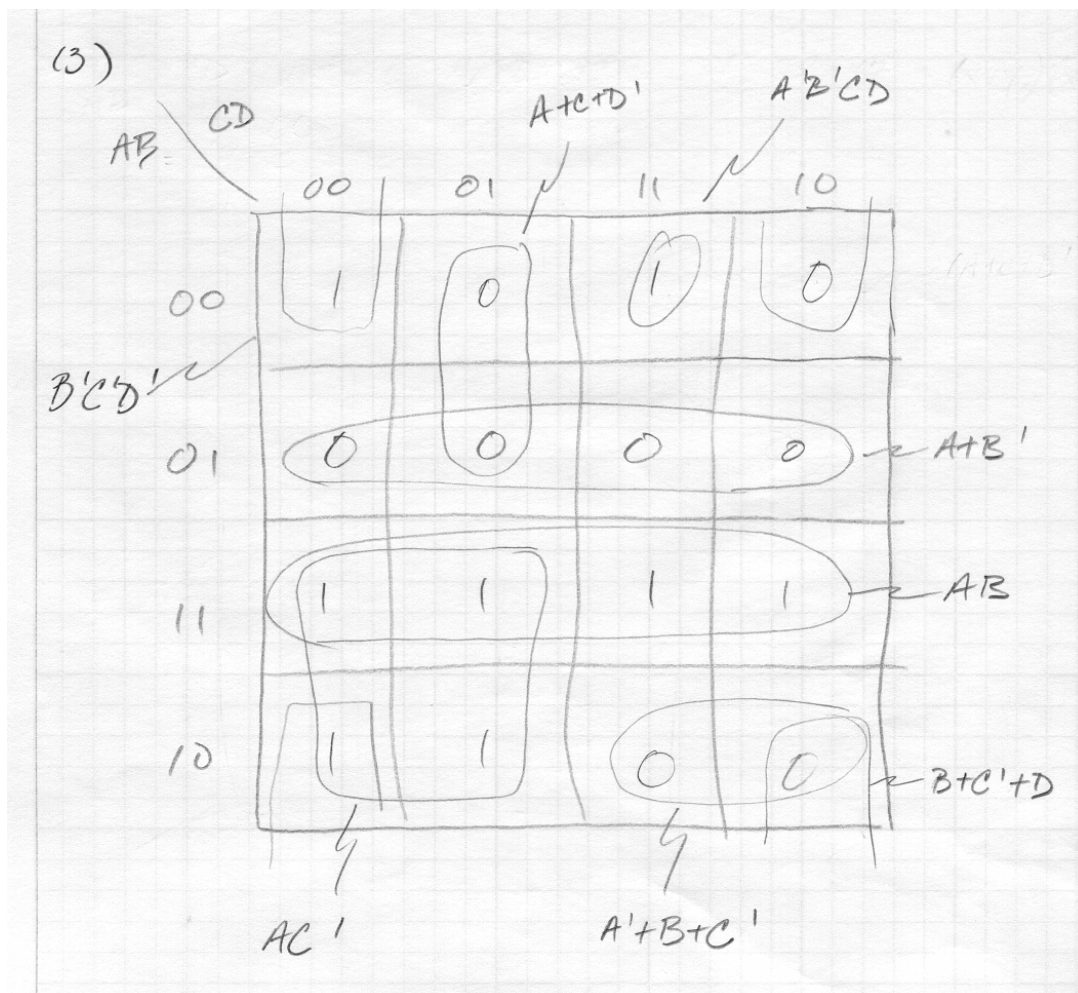
Problem #30.

For the function illustrated on the Karnaugh map below:

AB \ CD	00	01	11	10
00	1	1	0	1
01	0	0	1	0
11	1	0	0	0
10	1	0	1	1

(1) Determine the minimal (1) sum of products and (2) product of sums representations

SOP: $F = B'D' + A'B'C' + AC'D' + AB'C + A'BCD$

POS: $(A+B+C'+D')(A+B'+C)(A'+B'+D')$
$(A'+C+D')(B'+C'+D)$

... AMONG OTHERS

(2) In terms of prime implicants and essential prime implicants, are the representations unique and why or why not?

SOP IS UNIQUE BECAUSE COVER CONSISTS ENTIRELY OF ESSENTIAL PRIME IMPLICANTS

POS IS NOT UNIQUE BECAUSE ONLY ONE PRIME IMPLICANT IS ESSENTIAL AND THE REMAINDER OF THE COVER IS CHOSEN FROM SEVERAL POSSIBILITIES

Problem #31.

For the Karnaugh map shown below:

AB \ CD	00	01	11	10
00	0	X	0	0
01	X	1	X	X
11	1	1	0	1
10	1	1	0	X

(1) Express the function as both the canonical Sum-of-minterms and canonical Product-of-Maxterms (both in list form).

(1) $f = \Pi M (0,2,3,11,15) \cdot d(1,4,6,7,10)$

$f = \Sigma m (5,7,8,9,12,13,14) + d(1,4,6,7,10)$

(2) Find minimal sum of products and product of sums representations for the function.

(2) $f = (A+B)(C'+D')$

$f = A'B + AC' + AD'$

Note errors: 7 included on minterm list and don't care list
Minimal solution C'D + AD'

(3) What are minterm and maxterm lists for the function <u>as implemented</u> in part (2) above (where are the ones and where are the zeros) as opposed to the lists in part (1)?
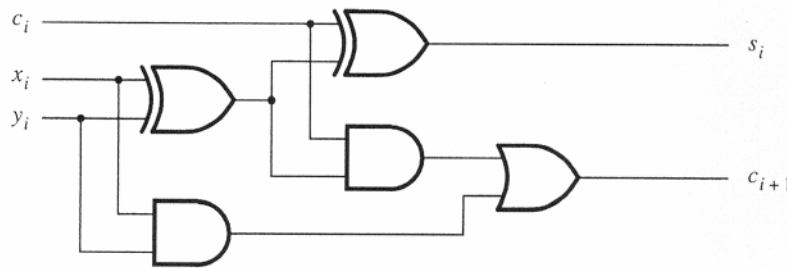
(3) $f = \Pi M(0, 1, 2, 3, 7, 11, 15)$

  $f = \Sigma m (4, 5, 6, 7, 8, 9, 10, 12, 13, 14)$

  ↑

  NOTE 7 ON BOTH LISTS

  ... INPUT IS DON'T CARE

<u>Problem #32.</u>

The figure bellows illustrates the construction of a full adder from two half adders.
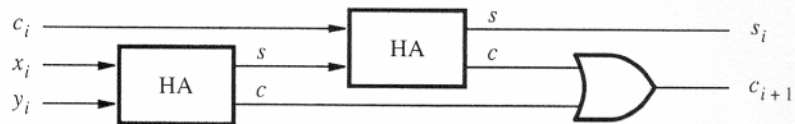
(a) Block diagram

(b) Detailed diagram

The propagation delays for the 7400 series AND, OR and XOR are given below:

		t_{PLH}	t_{PHL}
7486	XOR	30ns	22ns
7408	AND	27ns	19ns
7432	OR	15ns	22ns

(1) What are the propagation delays (high and low) from carry in to sum and carry out and what must the value of x and y be in order to "activate" these paths?

(1) $C_{IN} \rightarrow Sum$

$x = y = 0$, $C_{IN} \uparrow$ t_{PLH} (XOR) $= 30nS$

$x = y = 0$, $C_{IN} \downarrow$ t_{PHL} (XOR) $= 22nS$

$C_{IN} \rightarrow C_{OUT}$

$xy = 01$ or 10

$C_{IN} \uparrow$ t_{PLH} (AND) $= 27nS$

   t_{PLH} (OR) $= \underline{15nS}$

   $42nS$

$C_{IN} \downarrow$ t_{PHL} (AND) $= 19nS$

   t_{PHL} (OR) $= \underline{22nS}$

   $41nS$

(2) What are the propagation delays (high and low) from x to sum and carry out and what must the value of carry in and y be in order to "activate" these paths?

(3) What is the critical path (primary input to primary output) and what is the maximum propagation delay?

$x \rightarrow$ Sum

$C_{IN} = 0, \; y = 0$

$x \uparrow \quad t_{PLH} (XOR) = 30 \, nS$

$t_{PLH} (XOR) = \underline{30 \, nS}$

$60 \, nS$

$x \downarrow \quad t_{PHL} (XOR) = 22 \, nS$

$t_{PHL} (XOR) = \underline{22 \, nS}$

$44 \, nS$

$x \rightarrow$ CARRY OUT

$C_{IN} = 1$
$y = 0$

$x \uparrow \; t_{PLH} (XOR) = 30 \, nS$

$t_{PLH} (AND) = 27 \, nS$

$t_{PLH} (OR) = \underline{15 \, nS}$

CRITICAL PATH $\longrightarrow$ $72 \, nS$

$x \downarrow \; t_{PHL} (XOR) = 22 \, nS$

$t_{PHL} (AND) = 19 \, nS$

$t_{PHL} (OR) = \underline{22 \, nS}$ $\; 63 \, nS$

(4) Construct a timing diagram illustrating the delays along the critical path (showing all relevant internal nodes) and including both the sum and carry outputs.
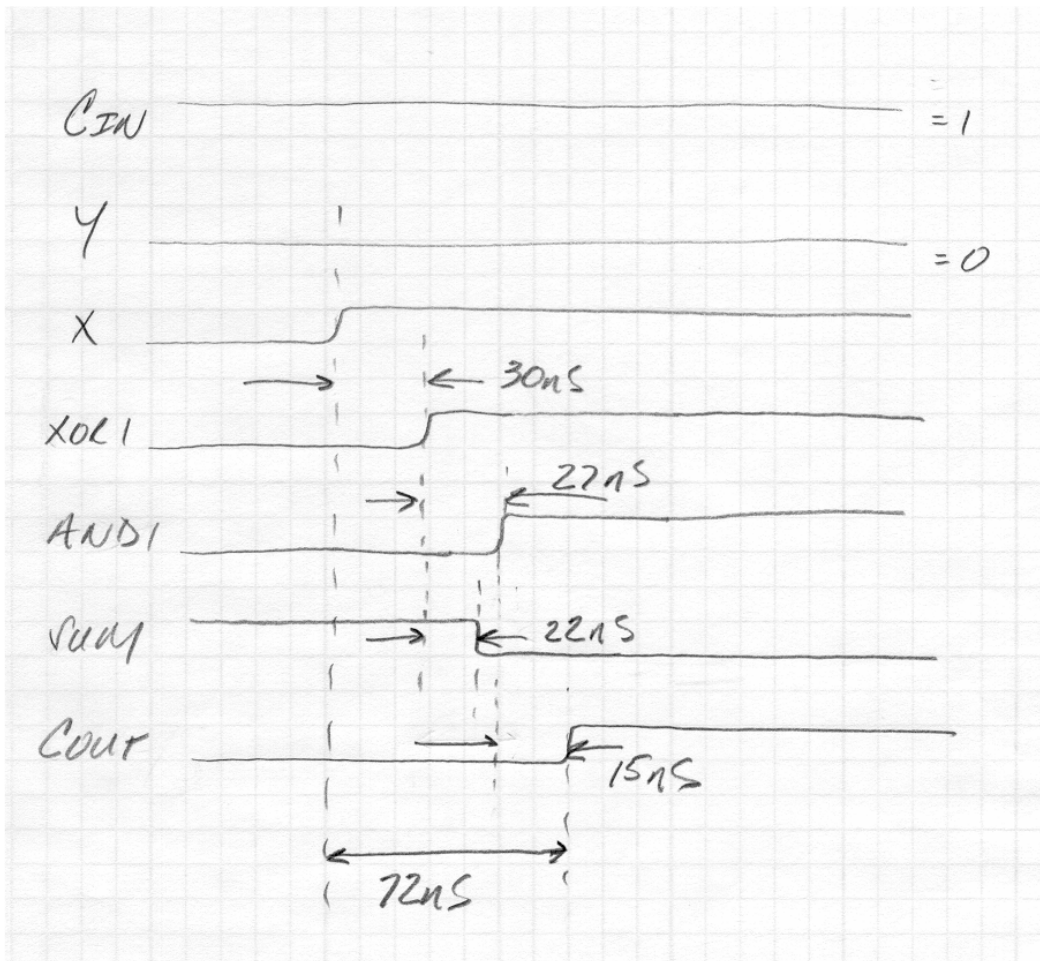
Problem #33.

In this problem you are to design a sensor and motor speed control circuit for a minivan's wheelchair lift system. The control system has 4 inputs and two outputs. The four inputs are (1) button internal (I), (2) button remote (R), (3) proximity detect (P) and (4) contact detect (C).   The two outputs are for motor speed (M1 M0) 00 = stop, 01 = slow, 11 = fast and 10 is not used. The direction of the motor is handled by a different circuit.

The proximity detector produces a logic 1 if an object is detected with 10 feet of the vehicle (and a 0 otherwise). The contact detector produces a 1 if actual contact is made with the vehicle or any portion of the lift. The button can be pressed from either inside the vehicle (internally) or remotely. If the button is pressed from inside the vehicle the proximity detector is a valid input; if remotely pressed, the proximity detector is ignored (though it still functions).

When the button is pressed internally the lift motor should operate at high speed. Should proximity be detected, the motor should slow and on contact the motor should stop. When operated remotely, the motor should never run at full speed and should stop on contact.

Construct a minimal product of sums implementation of this design using only NOR gates. State all of your assumptions clearly.

...MANY POSSIBLE INTERPRETATIONS
CONCERNING DON'T CARES...

IR \ CP	00	01	11	10
00	00	00	00	X
01	01	01	00	X
11	X	X	X	X
10	11	01	00	X

PLOT M_1, M_0 TOGETHER

I = INTERNAL
R = REMOTE
C = CONTACT
P = PROXIMITY

DON'T CARE CONDITIONS

① CONTACT = 1, PROXIMITY = 0

② INTERNAL = REMOTE = 1

K-map for M1:

IR \ CP	00	01	11	10
00	0	0	0	X
01	0	0	0	X
11	X	X	X	X
10	1	0	0	X

$$M1 = IP'$$

K-map for M0:

IR \ CP	00	01	11	10
00	0	0	0	X
01	1	1	0	X
11	X	X	X	X
10	1	1	0	X

$$M0 = C'(I + R)$$

Problem #34.

In this problem you are to design a portion of a display driver. The circuit takes as its input a four bit digit (D3:D0) plus a two bit input (I1:I0) indicating whether that digit is a BCD digit (I1I0 = 00), a hex digit (01), a one's complement number (10) or a two's complement number (11). The display you are driving has the usual segment inputs plus a single input which overrides the other inputs and causes an X should be displayed.

Design the circuit that drives the "display X" signal of the display. The circuit should output a logic 1 whenever an invalid input is detected and the number -0 should be considered invalid for this problem.

Use any technique you like and include your hardware implementation.

CONTROL INPUTS

    $00 \longrightarrow$ $1010, 1011, 1100, 1101, 1110, 1111$

    $01 \longrightarrow$ HEX, ALL VALID

    $10 \longrightarrow$ 1111 INVALID

    $11 \longrightarrow$ ALL VALID

WITHOUT DOING 6 VARIABLE K-MAP

- ALL 1's OCCUR WITH $I_1 I_0 = 00$ OR 01
- 1111 OCCURS ON BOTH PLANES

MAP FOR $I_1 I_0 = 00$

$$F = \overline{I_1}\,\overline{I_0}\,(D3 \cdot D2 + D3\,D1) + I_1 \overline{I_0}\,(D3 \cdot D2 \cdot D1 \cdot D0)$$

$$\text{OR } \overline{I_0}\,(D3 \cdot D2 \cdot D1 \cdot D0)$$

Note on Homework #2.
The problems above have been taken from previous midterms and homework. Additional midterm problems have been used as examples in class.   See presentation slides for more design examples (one's complement, BCD, hall light controller, adders, etc).